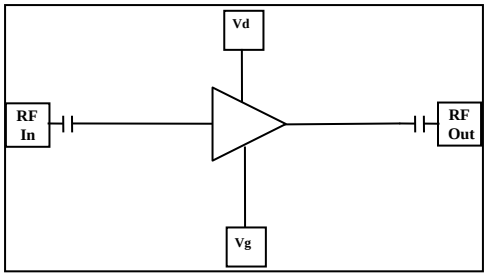
5 – 6 GHz 20dBm Gain block Amplifier

Features

- **Frequency Range : 5 – 6GHz**
- **21.5 dBm output P1dB**
- **14 dB Power gain**
- **30% PAE**
- **High IP3**
- **Input Return Loss > 12 dB**
- **Output Return Loss > 15 dB**
- **Dual bias operation**
- **No external matching required**
- **DC decoupled input and output**
- **0.5 µm InGaAs pHEMT Technology**
- **Chip dimension: 1.2 x 1.6 x 0.1 mm**

Functional Diagram



Typical Applications

- **RADAR**
- **Military & space**
- **LMDS, VSAT**

Description

The ASL4026 is a C-band Gain block amplifier with 20dBm power output. The PA operates in 5 – 6 GHz frequency range. The PA features 14 dB of gain with input and output return losses of 12 dB and 15 dB respectively. The PA has a high IP3 of 30dBm and 35% PAE. This feature enables it to be used in the applications requiring efficiency along with linearity. The chip operates with dual bias supply voltage. The die is fabricated using a reliable 0.5µm InGaAs pHEMT technology. The Circuit grounds are provided through vias to the backside metallization.

Absolute Maximum Ratings (1)

Parameter	Absolute Maximum	Units
Drain bias voltage (Vd)	+8	volts
Drain current (Idq)	120	mA
RF input power (RFin at Vd=9V)	23	dBm
Operating temperature	-50 to +85	^{o}C
Storage Temperature	-65 to +150	^{o}C

1. Operation beyond these limits may cause permanent damage to the component

Electrical Specifications [1] @ T_A = 25 °C, V_d = 8V, V_g = -0.9V, Zo =50 Ω

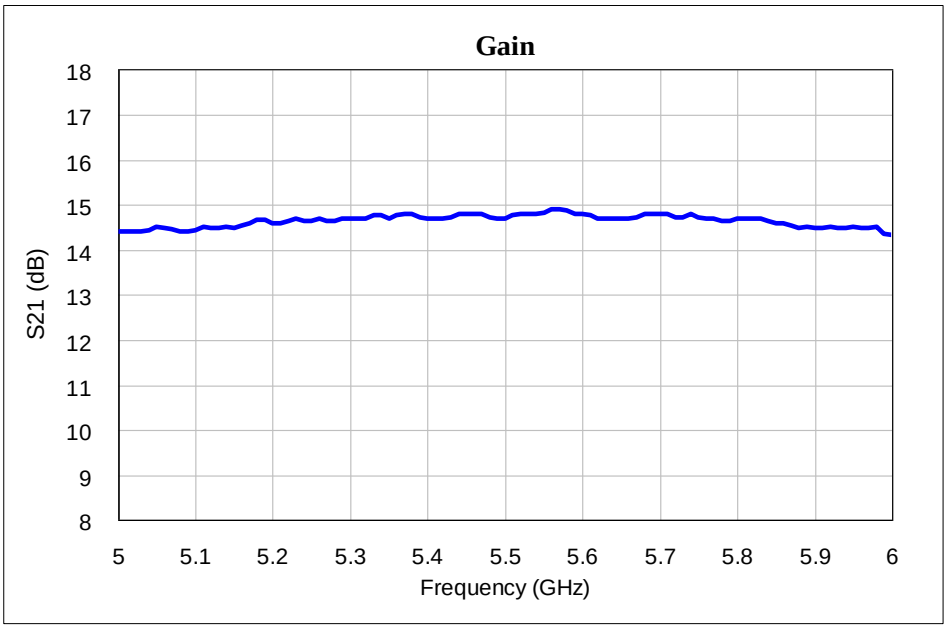
Parameter	Typ.	Units
Frequency Range	5 – 6	GHz
Gain	14	dB
Gain Flatness	+/-0.3	dB
Output Power (P1 dB)	21.5	dBm
Input Return Loss	12	dB
Output Return Loss	15	dB
Saturated output power (Psat)	22.5	dBm
Output Third Order Intercept (IP3)	30	dBm
Power Added Efficiency (PAE)	30%	--
Supply Current(Idq)	60	mA

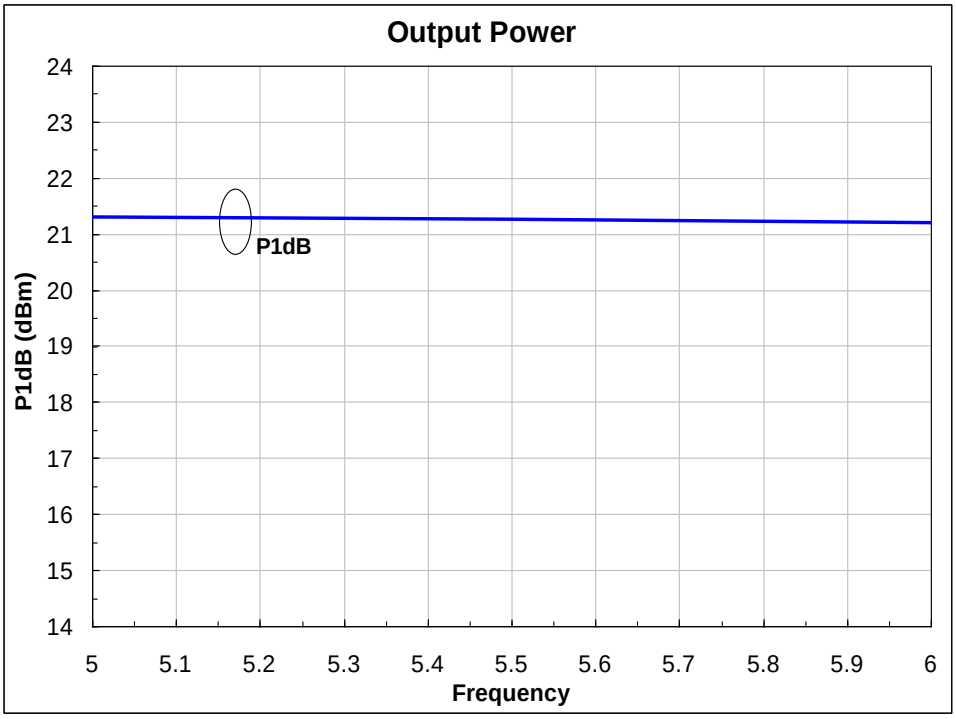
Note:

1. Electrical specifications as measured in test fixture.

Test fixture data

V_d = 8V, V_g = -0.9V, Total Current =60ma, T_A = 25 °C





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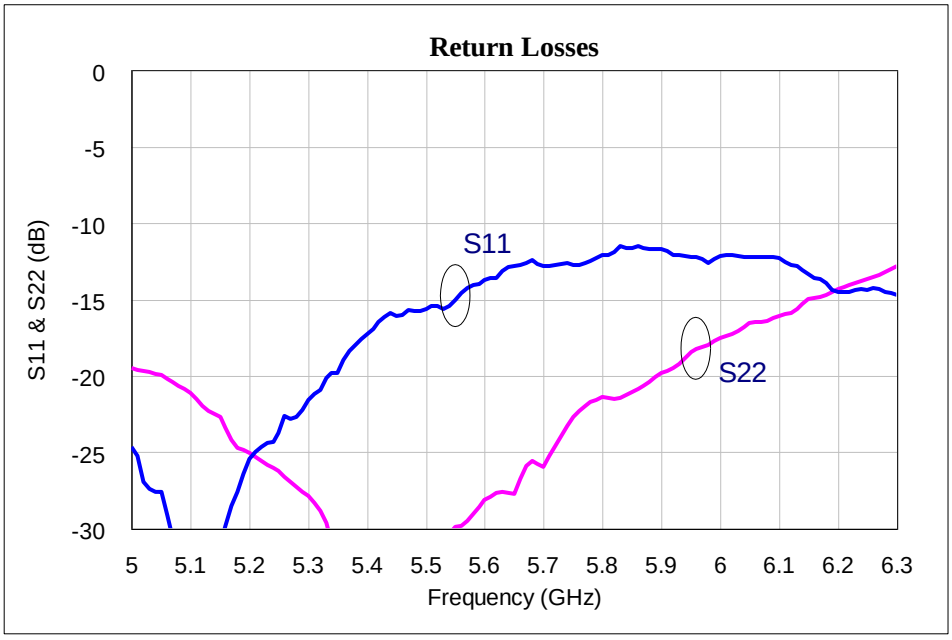
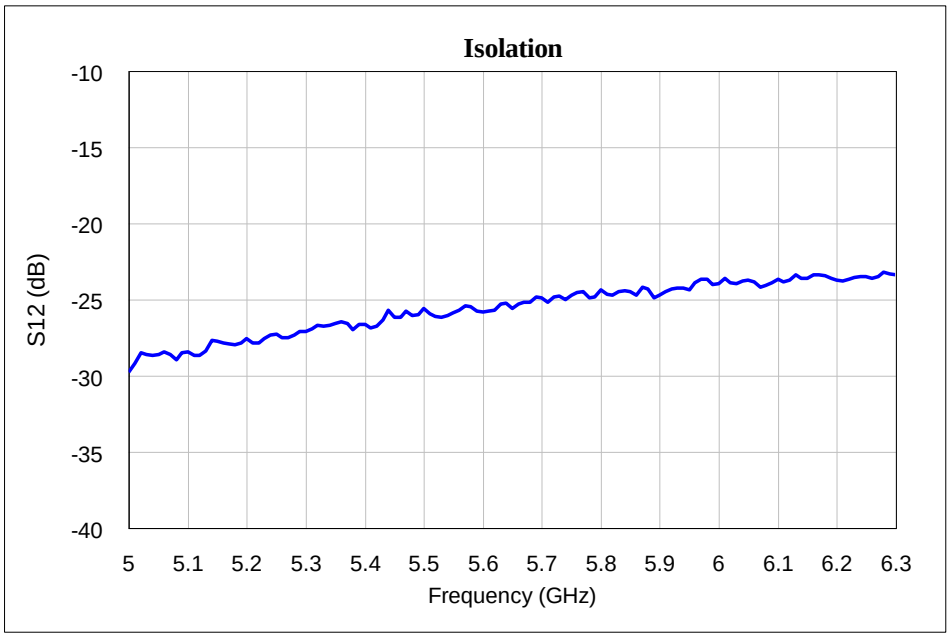
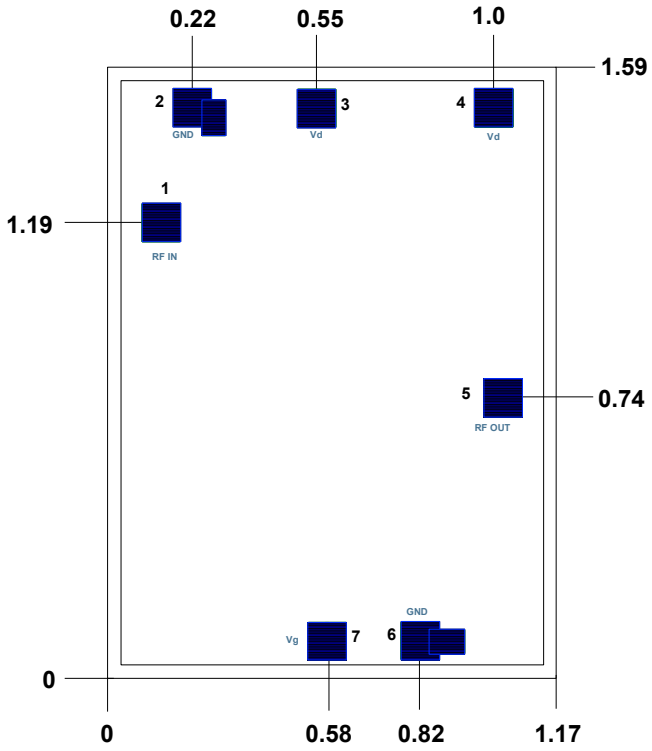




Bond Pad Locations

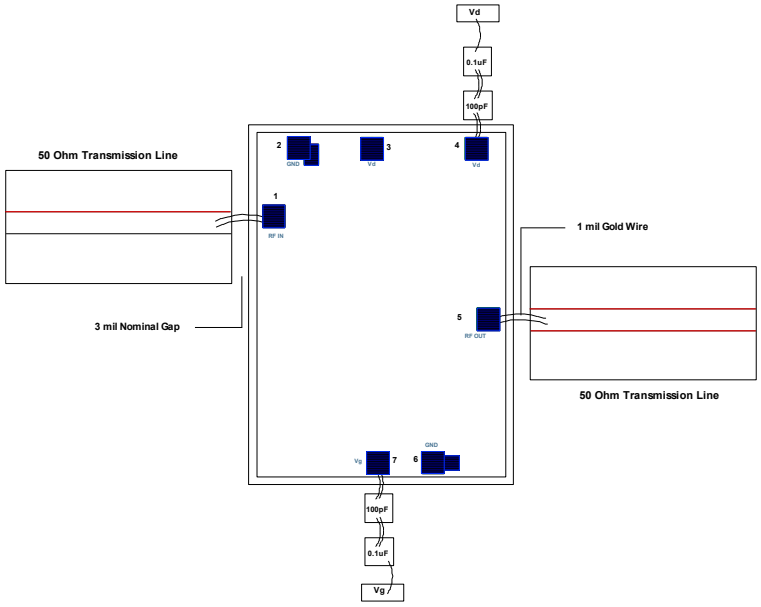


Units: millimeters

Note:

1. All RF and DC bond pads are 100µm x 100µm
2. Pad no. 1 : RF IN
3. Pad no. 4 : Drain voltage(V_d)
4. Pad no. 5 : RF Output
5. Pad no. 7 : Gate voltage (V_g)

Recommended Assembly Diagram



Note:

1. Two 1 mil (0.0254mm) bond wires of minimum length should be used for RF input and output.
2. Two 1 mil (0.0254mm) bond wires of minimum length should be used from chip bond pad to 100pF capacitor.
3. Input and output 50 ohm lines are on 5 mil RT Duroid substrate
4. 0.1 µF capacitors may be additionally used as a second level of bypass for reliable operation
5. The RF input & output ports are DC decoupled on-chip.
6. Proper heat sink like Copper tungsten or copper molybdenum to be used for better reliability of chip

Die attach: For Epoxy attachment, use of a two-component conductive epoxy is recommended. An epoxy fillet should be visible around the total die periphery. If Eutectic attachment is preferred, use of fluxless AuSn (80/20) 1-2 mil thick preform solder is recommended. Use of AuGe preform should be strictly avoided.

Wire bonding: For DC pad connections use either ball or wedge bonds. For best RF performance, use of 150 - 200µm length of wedge bonds is advised. Single Ball bonds of 250-300µm though acceptable, may cause a deviation in RF performance.

GaAs MMIC devices are susceptible to Electrostatic discharge. Proper precautions should be observed during handling, assembly & testing

All information and Specifications are subject to change without prior notice